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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/706,090

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Junji Sugamoto

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7590

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Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P.
1300 I Street, N.W.
Washington, DC 20005-3315

EXAMINER

LEE, GRANVILL D

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/706,090

Applicant(s)

SUGAMOTO ET AL.

Examiner

Granvill D Lee, Jr

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,7-17,20 and 22-25 is/are rejected.
- 7) ☒ Claim(s) 2,6,18,19 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/25/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claim 4 objected to because of the following informalities: The term “applying after-cleaning” is not clear or appears to lack a cleaning process step. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7, 14, 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Younan (Article V).

In view of these claims (esp. clm. 1 & 26), Younan treats a semiconductor wafer comprising, treating the semiconductor wafer (Abstr.) in a second solution called Secco etch, which includes at least one kind of an oxidative acid and an oxidizing agent, and treating the semiconductor wafer in a first solution including at least one of HF and NH₄F for 15 minutes (intro.)

In further view of claim 26, Younan discloses an in-test fabrication process where an apparatus is used wherein a first device to remove with a

chemical solution a film of a semiconductor wafer which may have a crystal defect, so as to expose a crystal surface of the semiconductor wafer: said film constituting a capacitor device structure including a device pattern; and a second device to selectively remove a surface layer of the semiconductor wafer by selective etching to bring the crystal defect into view (Abstr.). (Note, that the apparatus used is a fabrication process, which consists of some mechanism used to move and soak the wafers to be etched, as instant application fails to detail apparatus structure.)

In view of claim 7, Younan includes an oxidative hydrofluoric acid and a buffer oxide etchant (BOE) oxidizing agent (pg. 188 col. 2 para. 1).

In view of claim 14, Younan (Art. V) uses a chemical solution of HF and an buffer etchant (BOE) to remove residuals.

In view of claims 27 and 30, Younan (Art. V) uses a third etch step for 5 minutes (Pg. 188 col. 2, 3rd para.).

In view of claim 28 and 29 Younan (Art. V) uses two inspection steps using an optical inspection followed by a SEM inspection (Sect. III and fig. 2-4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

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skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3-5, 8-13, 15 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Younan (Article U).

In view of these claims, Younan treats a semiconductor wafer comprising, treating the semiconductor wafer (Abstr.) in a second solution called Secco etch, which includes at least one kind of an oxidative acid and an oxidizing agent, and treating the semiconductor wafer in a first solution including at least one of HF and NH₄F for 15 minutes (intro.). Note that Younan points out the first and second process solutions are identically opposite to the instant application, and therefore would be clear to one skilled in the art to consider rearrangement of a two-step chemical process, since process rearranging of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

In view of claim 3, Younan uses the Secco etch, which etches defective areas quicker than bulk areas of the semiconductor (pg. 20 col. 2 para.3).

In view of claim 4, Younan uses a HF deprocessing cleaning step first on the entire sample (pg. 21 col. 1 last para.-col. 2 third para.).

In view of claim 5, Younan suggests that HF has a 49% concentration (pg. 21 col. 1 last para.).

In view of claim 8, Younan discusses treating the wafer in a first solution of 49% HF, followed by an acid and HF solution (pg. 21 col. 1 last para.-col. 2 third para.).

In view of claims 9 and 23, Younan shows method of inspecting a semiconductor wafer which comprises a film constituting a device structure including a device pattern and which may have a crystal defect, the method comprising, removing said film with a chemical solution to expose the crystal surface of the semiconductor wafer, selectively removing a surface layer or the semiconductor wafer by selective etching to bring the crystal defect into view; and quantitatively evaluating the crystal defect (Abstr.). Younan further integrates the process and determines the causes of low-yielding manufacturing processes (pg. 22 col. 2 para. 2-5).

In view of claims 10-11 and 24, Younan further shows a chemical solution including a second solution having at least one kind of an oxidative acid and an oxidizing agent and a first solution having at least one of HF (pg. 20 Col. 2 para. 1-3).

In view of claims 12-13, 22 and 25, Younan continues with a process to reduce the residues with an agitated solution of the Secco etch solution.(pg. 21 col. 2 last para).

In view of claim 15, Younan uses a Secco etch solution of an oxidative hydrofluoric acid and a potassium dichromate oxidizing agent (pg. 20 col. 2 para. 1-3).

Claims 16-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Younan (Art. U) in view of Yasuo (Japan. Doc.11-054579).

In view of these claims, Younan shows method of inspecting a semiconductor wafer which comprises a film constituting a device structure including a device pattern and which may have a crystal defect, the method comprising, removing said film with a chemical solution to expose the crystal surface of the semiconductor wafer, selectively removing a surface layer or the semiconductor wafer by selective etching to bring the crystal defect into view; and quantitatively evaluating the crystal defect. But Younan analysis does not take into account creating a defect free pattern on the wafer to compare to the defective one as a reference.

Yasuo invents a method where a defect-free layer in a sample is created and used to compare to a sample with defects. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the Secco etch method of Younan with the substrate evaluation method of Yasuo to achieve better comparative results, since the crystals with defects are observed to create pits when etched and contrast well with those without the defects (Para. 0001-0006).

Claims 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Younan (Art. V) in view of Younan (Art. U).

In view of these claims, Younan (Art. V) shows method of inspecting a semiconductor wafer which comprises a film constituting a device structure including a device pattern and which may have a crystal defect, the method comprising, removing said film with a chemical solution to expose the crystal surface of the semiconductor wafer, selectively removing a surface layer or the semiconductor wafer by selective etching to bring the crystal defect into view, but fails to an ultrasonic wave generator to apply to the semiconductor. But, Younan (Art. U) continues with a process to reduce the residues with an agitated solution of the Secco etch (pg. 21 col. 2 last para). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the Secco etch method of Younan (Art. V) with the agitated method of Younan (Art. U) to achieve a cleaner sample, since it was desirable that bubbles or other by products should not remain on the surface (pg. 21 last para.- pg. 22 1st para.).

Allowable Subject Matter

Claims 2, 6, 18-19 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier

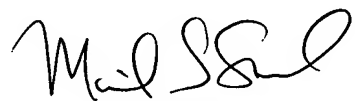
communications for the examiner should be directed to Granvill Lee whose telephone number is (571) 272-1897. The examiner can be normally reached on Monday thru Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Granvill Lee
Art Unit 2825

G1
9/1/04



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800